Q.P. Code: **16MC802** **R16**

Reg. No. | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
MCA I Year I Semester Regular & Supplementary Examinations Jan 2018
Computer Organization

Time: **3 hours** Max. Marks:**60**

(Answer all Five Units **5 X 12 = 60** Marks)

UNIT-I

1	a	Describe the importance of encoders	6M
	b	Describe full adder and its circuit diagram.	6M
		OR	
2	a	Explain JK flip-flop and T flip-flop.	6M
	b	Explain logical gates with their circuit diagrams.	6M

UNIT-II

3	a	Explain ROM and RAM.	6M
	b	Describe the importance of direct mapping.	6M
		OR	
4	a	Briefly explain the micro programmed control.	6M
	b	Explain Auxiliary memory.	6M

UNIT-III

5	a	Describe data transfer instructions.	6M
	b	Explain shift and rotate instructions.	6M
		OR	
6	a	What is address transfer and explain it clearly?	6M
	b	Describe the Flag transfer.	6M

UNIT-IV

7	a	What is interrupt and explain with suitable example?	6M
	b	Describe interrupt cycle?	6M
		OR	
8		What is DMA? How the DMA controller works?	12M

UNIT-V

9	a	Explain shared memory multiprocessors?	6M
	b	Describe the inter processor communication.	6M
		OR	
10	a	What is parallel processing?	6M
	b	Explain RISC pipeline.	6M

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